UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/287,304	04/07/99	YAMAMOTO	A 0941.63012

024978
GREER, BURNS & CRAIN
300 S WACKER DR
25TH FLOOR
CHICAGO IL 60606

WM01/0201

EXAMINER	
PIZIALI,J	
ART UNIT	**PAPER NUMBER**
2673	5

DATE MAILED:
02/01/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/287,304	YAMAMOTO ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 April 1999* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Drawings

1. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Youn (5,856,816).

Regarding claim 1, Youn discloses a liquid crystal display device comprising an LCD panel [Fig. 2, 1]; a data driver [Fig. 3] connected to the LCD panel; a gate driver [Fig. 2, 3] connected to the LCD panel; and the data driver being divided into a plurality of blocks, which simultaneously supply the LCD panel with display signals respectively supplied thereto (Column 1, Line 10 - Column 2, Line 20).

Regarding claim 2, Youn discloses a block comprising a shift register [Fig. 5, 21]; signal lines [Fig. 5, Y] to which the display signals are supplied; data bus lines connected to the signal lines and the LCD panel; and analog switches [Fig. 5, 29-30] provided in the data bus lines and controlled by an output signal of the shift register thereto (Column 4, Line 39 - Column 5, Line 38).

Regarding claim 3, Youn discloses a driver device [Fig. 5, 22-23] which receives display data [Fig. 5, D] externally supplied and outputs the display signals derived therefrom to the blocks of the data driver (Column 4, Line 39 - Column 5, Line 21).

Regarding claim 4, Youn discloses a plurality of driver devices [Fig. 5, 22-23] which are respectively associated with a plurality of ones of the blocks, each of the plurality of driver devices receiving display data [Fig. 5, D] externally supplied and outputting the display signals derived therefrom to associated blocks of the data driver (Column 4, Line 39 - Column 5, Line 38).

Regarding claim 5, Youn discloses the display signal lines of the associated blocks have parts extending from one of the plurality of driver devices through a space located between the associated blocks [Fig. 5].

Regarding claim 6, Youn discloses a substrate on which the LCD panel, data driver and gate driver are integrally formed (Column 1, Lines 10-20).

Regarding claim 7, Youn discloses the data driver comprises polysilicon transistors (Column 1, Lines 10-20).

Regarding claim 8, Youn discloses a display signal supply device [Fig. 5, 22-23] which outputs the display data [Fig. 5, D] to the driver device (Column 4, Line 39 - Column 5, Line 21).

Regarding claim 9, Youn discloses the display signal display device is formed on the LCD panel (Fig. 1; Column 1, Line 10 - Column 2, Line 20).

Regarding claim 10, Youn discloses a display signal supply device [Fig. 5, 22-23] which outputs the display data [Fig. 5, D] to the plurality of driver devices (Column 4, Line 39 - Column 5, Line 21).

Regarding claim 11, Youn discloses each of the plurality of blocks supplies the LCD panel with a given number of display signals at once (Column 4, Line 39 - Column 5, Line 38).

Regarding claim 12, Youn discloses the driver device comprises a shift register [Fig. 5, 21] which outputs a shift signal, first latch circuits [Fig. 5, 22-23] which latch the display data in response to the shift signal, and second latch circuits [Fig. 5, 25-26] which latch the display data from the first latch circuits in response to a latch enable signal externally supplied (Column 4, Line 39 - Column 5, Line 38).

Regarding claim 13, Youn discloses digital-to-analog converters [Fig. 5, 27-28] which convert the display data from the second latch circuits into analog signals (Column 5, Lines 4-13).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Callahan Jr. et al. (5,574,475), Kawamori (5,598,178), Dingwall (5,739,805) and Tsuzuki et al. (5,745,093) are cited to show the state of the art in respect to driving liquid crystal displays.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-6606 for regular communications and (703) 308-9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

J.P.
January 29, 2001

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600